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Search History

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L4	redundant adj3 line	1639	L4
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L2	memory	441408	L2
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END OF SEARCH HISTORY

L8: Entry 1 of 3 File: USPT Nov 11, 2003

DOCUMENT-IDENTIFIER: US 6646912 B2
TITLE: Non-volatile memory

Detailed Description Text (58):
Another possible usage of redundant sense lines is to check the function of the memory before it is written. Information maybe gathered from inconsistent measurements from various sense lines in combination with various states of the power supply connections to the row and column electrode ends to reveal defective memory elements and/or defective addressing. This information maybe used to generate sparing tables that can be used to avoid writing to defective areas of the memory module and thereby improve the product tolerance to processing yields

(b) an address conversion unit which converts the X and Y addresses of said failures detected by said failure determining means into addresses of said compressed data matrix storage device and controls the storing of failure data in said compressed data matrix storage device;

(c) an auxiliary processing unit which judges whether remedy of the failures is possible on the basis of the data of the test results stored in said compressed data matrix storage device and for controlling said remedying means when remedy of the failures is not possible;

(d) means for selecting said redundant lines by analyzing the data in said compressed data matrix storage device and for supplying the identify of said redundant lines to said remedying means; and

(e) means for supplying the data in said compressed data matrix storage device to said remedying means.

storage device, the defect stack storage device is processed. The column select lines which exceed a certain number of errors are determined and stored in the stack storage device 42. For this purpose, corresponding CSL defect counters 31 are incremented. In this architecture, there is one defect counter for each column select line of the memory region to be tested. The defect counters for the respective column select lines are activated whenever new defect addresses are written to the defect storage device from the buffer storage device. If one of these defect counters overflows, then the corresponding column select line address is stored in the stack storage device 42. In addition, it is necessary to clear the associated entries, that is to say the column select line address and the word line address, from the defect stack storage device, since the defects are now repaired by the use of a redundant column select line. Moreover, the associated redundancy counter is incremented. This procedure ensures that acceptable test results are indeed obtained even with the integration of a relatively small defect stack storage device. If the defect stack storage device overflows, it is not possible to repair the chip with the aid of this method and the built-in self-test can be immediately terminated at this point. Once the test sequence is ended, the content of the defect stack storage device has to be evaluated. In order to evaluate the defect stack storage device, the method explained with regard to the second exemplary embodiment can be used, for example.

L13: Entry 2 of 7 File: USPT Jul 9, 2002

DOCUMENT-IDENTIFIER: US 6418069 B2
TITLE: Method of repairing defective memory cells of an integrated memory

Brief Summary Text (19):
upon finding a defect of the memory cell being tested, the affected column line is replaced with one of the redundant column lines if a number of the programmed redundant column lines does not exceed a threshold value;

Brief Summary Text (24):
In this embodiment, a repair of detected defects in each case takes place perpendicularly to the direction of testing. This is because testing takes place row by row and replacement initially takes place column by column. It is only when the number of the redundant column lines already used exceeds the limit value that the preceding programming operations are at least partially canceled. However, it is only the programming operations of those redundant column lines which have been programmed on the basis of defects recognized in the relevant row line which are being canceled. Since the row line affected is then replaced by a redundant row line and the programming of redundant column lines which has taken place on the basis of row lines previously tested is not canceled, all defects detected are repaired in the manner described within a single test run through the memory cells if there are sufficient redundant lines.

Detailed Description Text (2):
Referring now to the figures of the drawing in detail and first, particularly, to FIG. 1 thereof, the memory cells of the integrated memory are successively tested. To test the next memory cell in each case, the address is correspondingly incremented. With each beginning of the testing of a new row line, a counter X is set to zero. If a defect is detected, the counter X is incremented by one and the count of the counter X is compared with a limit value Y. The limit value Y applies to the number of maximum column lines permitted and programmed for the repair in the current row line. This is because the memory cells are tested row by row whereas the repair is carried out column by column when a defect is found. As long as the counter X does not exceed the limit value Y when a defect is found, the defect is eliminated by a redundant column line. If, however, the counter X exceeds the limit value Y, the programming of the redundant column lines which have been programmed for the repair of defects detected in the current row line is canceled. After that, the current row line is repaired by a redundant row line.

Detailed Description Text (3):
It is particularly advantageous if the redundant row line acting as replacement itself is checked for errors after the replacement. For this purpose, the repair method is continued with the check of the memory cell of the redundant row line which has the lowest column address. If errors are detected on the redundant row line, a repair is initially effected via the redundant column lines as before. If their number exceeds the permissible limit value, their programming is canceled and the redundant row line is replaced by another redundant row line. Naturally, the checking of the memory cells of a programmed redundant row line can be omitted if the redundant lines have been tested before they were programmed and only error-free redundant lines are subsequently used for a repair.

Detailed Description Text (5):
The left-hand part of FIG. 11 also shows the manner in which the defective memory cells MC have been repaired. To the right of the memory cell array, the redundant bit lines RBLi programmed for replacing the respective normal bit lines BL have been entered and below the memory cell array, the redundant word lines RWLi programmed for replacing the normal word lines are entered. In the present case, a sequential test of the memory cells MC has already taken place before the state shown in FIG. 11, beginning with memory cell address 0,0 (that is to say word line WL0 and bit line BL0) in the direction of the word lines WL. Memory cell 0,0 does not exhibit a defect. After that, memory cell 0,1 was tested (word line WL0, bit line BL1) and a defect was found. This defect was repaired by replacing the bit line 1 with the redundant bit line RLB0. After that, testing of the memory cells continued and, at the beginning of the next word line WL1, the error counter X was reset to zero. The defective memory cell 1,0 on word line WL1 was repaired by the redundant bit line RBL1 and the error counter X was incremented to the value 1. Since bit line BL1 has already been replaced by the redundant bit line RBL0, the next error found is the one having the address 1,2. This is repaired by means of the redundant bit line RBL2. The error counter X is incremented to 2. Next, the defect of memory cell 1,3 is found. This state is shown in FIG. 11. This defect is not repaired by means of a redundant bit line since the error counter X is increased to three and has thus exceeded the limit value Y which also has a value two. In consequence, the programming of the redundant bit lines RBL1 and RBL2 which have been found at addresses 1,0 and 1,2 on the basis of the defects found in the current word line WL1, is canceled. In contrast, the programming of the redundant bit line RBL0 which replaces the normal bit line BL1 is not canceled since it did not take place due to a defect detected in the current word line WL1. Its programming took place on the basis of the defect with address 0,1, found in the word line WL0. After that, the normal word line WL1 is replaced by the redundant word line RWL0.

Detailed Description Text (6):
FIG. 12 shows this state of the integrated memory. The limit value Y is again set to the value 2 since two of the redundant bit lines RBLi are again available for programming. These are redundant bit lines RBL1 and RBL2, the programming of which has been canceled as has just been described. The memory cells are continuously tested so that next the defect having address 3,0 is detected. This is again repaired by means of one of the redundant bit lines RBLi. The repair method is analogously continued, the programming of some of the redundant bit lines being canceled whenever the count of counter X exceeds the limit value Y.

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L13: Entry 7 of 7 File: USPT Jun 14, 1988

DOCUMENT-IDENTIFIER: US 4751656 A
TITLE: Method for choosing replacement lines in a two dimensionally redundant array

Detailed Description Text (4):
Following compilation of the bit failure map, in a step 20, the bit line scan is begun with the scan direction scanning down the bit lines 10. In a step 22, the next word line 12 from bit lines 0 to 13 is tested and the number of failures in that word line are counted. In a test 24, the number of failures is compared against a bit scan limit. Initially, the bit scan limit is set to the number of redundant bit lines, 2 in the example. If the number of failures exceeds the bit scan limit, then a fail has been detected. In the example, the initial value of the bit scan limit is 2. Only those word lines containing greater than two failures are detected as fails. If no fail has been detected, then a test 26 determines if all the word lines have been tested. If not, the next word line is stepped to. At the end of the bit line scan 26, a test 28 is made to determine whether there have been any failures of word lines exceeding the bit scan limit. If not, a test 30 determines if both the bit scan limit and a word scan limit, to be described later, are equal to zero. If so, the memory chip is noted as being at least fixable. If both scan limits are not zero, then the bit scan limit is reduced by one in step 32 and the procedure is repeated with the reduced bit scan limit.

L14: Entry 11 of 13 File: USPT Jul 28, 1992

DOCUMENT-IDENTIFIER: US 5134616 A
TITLE: Dynamic RAM with on-chip ECC and optimized bit and word redundancy

Detailed Description Text (33):
In the chip described here, the error correction affects only a single failing bit in an error correcting code word. Any additional faults in an error correcting code word must be fixed with redundancy or else the chip will fail. In order to optimize the fault tolerance of a chip with error correction, it is necessary to replace the multiple faults in an error correcting code word in a systematic way. The first step in achieving this is by the use of the bit line redundancy of the invention, wherein two blocks within each quadrant have their own redundant bit lines that can substitute any defective bit therein. Based on computer simulations and theoretical calculations, the fault tolerance of the ECC increases dramatically by this use of the redundant bit lines of the invention.

Detailed Description Text (34):
As shown in FIG. 13, without the use of the error correcting code circuits, (i.e. using redundant bit lines only), an average of 28 randomly failing single cells per chip would result in an expected yield of 50% for a 16 Mb chip. Using the error correcting code circuits only, with no bit line redundancy, results in a 50% yield for an average of 428 random single cell failures per chip, as previously described. Combined use of the bit line redundancy of the invention and error correcting code produces a 50% yield at an average of 2725 randomly failing single cells per chip. It was also found theoretically that the fault tolerance increase depended sharply on the number of redundant bit lines per segment. Hence, while two redundant bit lines per segment is given by way of example, as a practical matter more lines could be added to increase the reliability results. In the invention two redundant bit lines were used because even greater fault tolerance optimization could be achieved by the use of the redundant word line techniques of the invention.

L19: Entry 2 of 28 File: USPT Mar 25, 2003

DOCUMENT-IDENTIFIER: US 6539506 B1
TITLE: Read/write memory with self-test device and associated test method

Brief Summary Text (3):
The invention relates to devices and methods for testing read/write memories with integrated redundancy in which test patterns are written to a memory array and subsequently read out and compared and, if possible, until no more defects are present, as long as word lines and column select lines are replaced by redundant lines.

Detailed Description Text (3):
Referring now to the figures of the drawings in detail and first, particularly, to FIG. 1 thereof, there is seen a block diagram of a self-test architecture integrated in the memory chip and serving for repairing a memory module using existing line redundancy. The method which is realized by the architecture is iterative, that is to say it requires a plurality of test passes in order to determine the redundancy lines to be activated. A test pass includes all test patterns which are provided for the corresponding memory chip during a so-called prefuse test. Test patterns can be read into a memory array by a control unit CTRL containing a read-only memory ROM, for example. A memory array 1 in this case corresponds to a region of an overall memory array to which a certain number of redundant lines are assigned. The control unit CTRL performs an entire sequence control and can be supplied with external data. The memory array 1 has a plurality of word lines WL and a plurality of column select lines CSL and a content of the memory array is compared with the written-in test patterns by a comparator 21. Furthermore, the comparator 21 carries out a comparison of the defect address in the form of word line and column select line with defect addresses stored in corresponding stack storage devices 41 and 42. A defect address ascertained in the comparator 21 is available to defect counters 31 in a counter array 3. Moreover, redundancy counters 32 are provided in the self-test device. Values of the defect counters can be compared in a comparator 22.

Detailed Description Text (6):
Before the respective defect counters of a defective line are incremented, it is necessary to check whether the word line or column select line address of the defect is already stored in the associated stack storage device. In this case, the counters are not activated since the defect is already repaired. This comparison must be made as early as in the first test pass because a pass is formed of a plurality of test patterns. This prevents a defect from being rectified by a plurality of redundant lines. The addresses of the lines having defect counters that have overflowed after the first test pass are stored in the word line stack storage device 41 or in the column select line stack storage device 42, respectively. In addition, the associated redundancy counters 32 are incremented. For this purpose, it is necessary to determine the domain of the line to be replaced, because there are usually a fixedly prescribed number of redundancy lines for each word line domain and for each column select line domain of a memory chip. The memory array 1 constitutes a memory region which in turn includes WL and CSL domains. The redundancy counters are advantageously constructed in such a way that an appropriate redundancy line is no longer present in the event of an overflow. The memory module is thus non-repairable and the test can be immediately ended in

this case.

CLAIMS:

8. The method for testing a read/write memory according to claim 7, which further comprises: a) initially setting defect counters and redundancy consumption counters to zero; b) comparing an information item written to a memory array and an information item read from the memory array and ascertaining a defective cell; c) checking an address of the word line and an address of the column select line associated with the defective cell to determine if the address of the word line and the address of the column select line associated with the defective cell are already stored and incrementing the defect counter associated with the respective word line only when the address of the word line has not yet been stored and incrementing the defect counter associated with the respective column select line only when the address of the column select line has not yet been stored; d) storing addresses of at least one of the word line and the column select line and incrementing the associated redundancy consumption counter if the associated defect counters exceed a repair threshold; e) carrying out steps b) to d) for all prescribed test patterns and all of the cells of the memory array or until the redundant lines have been consumed; f) setting all of the defect counters to zero; g) carrying out step b); h) carrying out step c); i) separately determining the word line and the column select line with the largest number of defects, with comparators and the defect counters; j) selecting one of the word line and the column select line with the largest number of defects; k) storing the address of the selected line with the largest number of defects and incrementing the redundancy consumption counter if a number of remaining redundant lines exceeds a still-required number of lines; l) carrying out step k) with the other of the lines selected according to step i) if no more redundant lines are present for the line selected according to step j); m) terminating a test if the corresponding redundancy has been consumed; n) repeating steps f) to m) for all prescribed test patterns and for all of the memory cells of the memory array; and o) repeating step n) until no more defects in the memory array are used or the redundant lines have been used up.

L19: Entry 20 of 28 File: USPT Jan 6, 1998

DOCUMENT-IDENTIFIER: US 5706234 A
TITLE: Testing and repair of wide I/O semiconductor memory devices designed for testing

Detailed Description Text (3):
A procedure, or process, is used for testing a device and for determining a repair scheme that designates certain defective lines for replacement by redundant lines. This procedure includes the following. Enabling a test mode of the device under test 40. Performing DC electrical tests on the device under test to verify proper electrical contact and device operating characteristics. Systematically addressing the memory cells of the device and storing a pattern of test data bits into the memory cells of the device under test. Systematically addressing the memory cells and reading the stored test data bits from memory cells of the device under test. Comparing the data bits read from the device under test with one another and with the expected data bits, generated by the memory device tester, to identify defective cells. Storing cell address and test result information in the device tester 30.

L19: Entry 11 of 28 File: USPT May 16, 2000

DOCUMENT-IDENTIFIER: US 6065134 A
TITLE: Method for repairing an ASIC memory with redundancy row and input/output lines

Brief Summary Text (10):
A conventional solution provides repairing schemes that encompass a number of separately performed processes, each of which requires equipment that is external to the ASIC memory chip. The first of these processes is testing. Automatic Test Equipment (ATE) is used to test at least one memory array on an ASIC chip. A series of test signal patterns is applied through the ATE to detect the locations of memory failures based upon responsive outputs which are then recorded in the ATE. The next process is one of analysis. External software is used to determine optimal utilization of the redundant memory lines to repair the defective memory lines. The third process is the repair process. Fuse and/or antifuse equipment facilitates severing circuit fuses that are formed on the chip for selective removal through conventional laser beam techniques to repair a defective memory cell. The final process involves retesting the chip using the ATE to ensure that the chip functions properly after being repaired. The repaired chip is then packaged and sent to the customer.

Detailed Description Text (2):
Referring now to FIG. 1, there is shown a block diagram of a system 10 for testing and repairing configurable ASIC memories. System 10 comprises a memory array 30, a built-in self-test (BIST) circuit 22, and a fault-latching-and-repair-execution (FLARE) circuit 25. Memory array 30 contains a matrix of row memory lines intersecting I/O memory lines for storage logical data represented in binary format at the intersections of row memory lines and I/O memory lines. BIST 22 is coupled to memory array 30 to test for defective row and I/O memory lines, if any, in memory array 30. BIST 22 contains a test pattern generator 23 for generating different test patterns to verify the integrity of a memory cell. FLARE 25 is coupled to memory array 30 to repair defective row and I/O memory lines by redirecting the original address locations of defective memory lines to the mapped address locations of redundant or redundancy memory lines. FLARE 25 contains a row self-repair circuit 26 for repairing row memory lines and an I/O self-repair circuit 27 for repairing I/O memory lines. The decision to repair a faulty row or I/O memory line by FLARE circuit 25, as later described herein, depends on a dominant fault mechanism selected for implementing the repairing method.

L19: Entry 8 of 28 File: USPT Feb 6, 2001

DOCUMENT-IDENTIFIER: US 6185709 B1
TITLE: Device for indicating the fixability of a logic circuit

Brief Summary Text (4):
The combination of memory with logic on the same chip, particularly where DRAMs are used for the memory device, produces significant manufacturing problems. For instance, the DRAM cells are sensitive to minor defects that the more durable logic will withstand. The logic may require extra wiring layers to allow tightly packed logic cells to be interconnected. The wiring necessary for the logic may, however, impair transmitted signal margins, and otherwise decrease chip yield. An additional serious consequence is the effect of testability of a chip having the embedded memory. On-board Built-In Self Test (BIST) circuitry is provided to produce a set of complex data patterns, address sequencing, and control signals to check the logic circuitry and connected memory elements. The BIST circuitry includes logic circuitry which is used to identify failed memory cells, and to allocate replacement memory cells for the failed cells. In an embedded DRAM the results of testing word lines of memory cells, as well as column lines of memory cells may be provided to the allocation logic circuit to identify failed memory cells. Faulty word line addresses are stored in a wordline register, and redundant word line memory cells in the DRAM are assigned to replace the failed wordlines by the allocation logic. The fixability of the DRAM macro, i.e., the ability to replace all defective memory cells with redundant memory cells, may be determined from an overflow bit in the register storing the faulty word line addresses. If there is an overflow bit, indicating that more word line memory elements have failed than can be replaced by redundant memory word line elements, the inability to fix the embedded DRAM is easily determined by a connected tester which monitors the overflow bit.

L19: Entry 28 of 28 File: USPT Dec 9, 1986

DOCUMENT-IDENTIFIER: US 4628509 A
TITLE: Testing apparatus for redundant memory

Detailed Description Text (3):
(1) The possibility of remedy using the redundant lines incorporated in the memory under test (such as that indicated by reference numeral 3 in FIG. 1) is judged while the test is being conducted, whenever the comparator (indicated by reference numeral 4) outputs a failure result, and no remedy processing is carried out for any memory for which remedy is judged to be impossible on the basis of the failure pattern and number of failures generated up to that time. In other words, that memory is judged to be "NG" (no good), and subsequent failure results are not input for it. On the other hand, the testing is continued to the end for those of the memories for which an analysis of the remedy judgement indicates the possibility of remedy, even if failure data has been input for them. After the test is completed, judgement processing of the remedy lines is conducted on the failure data remaining in compressed matrix form, to provide an analysis for remedy judgement.

Detailed Description Text (38):
As described above, this embodiment compresses the analysis data for the remedy judgement into a matrix of only 6.times.6, which is determined by the number of redundant lines, simultaneously with completion of the test, irrespective of the size of the memory under test, and can drastically reduce the time required for reading and analyzing the data. During the test, too, this embodiment makes it possible to identify those memories being tested for which a remedy is not possible, and redundant lines can be decided on without the need of analysis, depending upon the pattern of the failure occurrences. This also results in a reduction of the analysis time. Moreover, in comparison with the prior art which uses a memory of the same capacity as that of the memory being tested as a failure memory, the embodiment makes it possible to greatly reduce the hardware construction because it is constituted by the compressed data matrix 17 of an extremely small capacity, and 1-bit wide memories, such as the failure line registers XFLRs 20, 21, the failure counters XLFC 24, YLFC 25, the address registers XAR 33, YAR 34, etc. Various matrix sizes can be realized easily according to the number of redundant lines, in the same way as in this embodiment.

CLAIMS:

1. In an apparatus for testing a redundant memory including means for applying a test pattern to a memory under test which has a matrix of storage cells having X and Y addresses, means for determining failures in the data stored in the storage cells of said memory on the basis of test results obtained by comparing outputs from said memory under test with expected values, and means for remedying said failures along selected redundant lines in the X and/or Y directions of said matrix of storage cells, the improvement comprising:

(a) a compressed data matrix storage device for storing as compressed data only the data relating to failures determined from the test results of said failure determining means;

L9: Entry 1 of 1 File: USPT Mar 25, 2003

DOCUMENT-IDENTIFIER: US 6539506 B1
TITLE: Read/write memory with self-test device and associated test method

Detailed Description Text (3):
Referring now to the figures of the drawings in detail and first, particularly, to FIG. 1 thereof, there is seen a block diagram of a self-test architecture integrated in the memory chip and serving for repairing a memory module using existing line redundancy. The method which is realized by the architecture is iterative, that is to say it requires a plurality of test passes in order to determine the redundancy lines to be activated. A test pass includes all test patterns which are provided for the corresponding memory chip during a so-called prefuse test. Test patterns can be read into a memory array by a control unit CTRL containing a read-only memory ROM, for example. A memory array 1 in this case corresponds to a region of an overall memory array to which a certain number of redundant lines are assigned. The control unit CTRL performs an entire sequence control and can be supplied with external data. The memory array 1 has a plurality of word lines WL and a plurality of column select lines CSL and a content of the memory array is compared with the written-in test patterns by a comparator 21. Furthermore, the comparator 21 carries out a comparison of the defect address in the form of word line and column select line with defect addresses stored in corresponding stack storage devices 41 and 42. A defect address ascertained in the comparator 21 is available to defect counters 31 in a counter array 3. Moreover, redundancy counters 32 are provided in the self-test device. Values of the defect counters can be compared in a comparator 22.

Detailed Description Text (6):
Before the respective defect counters of a defective line are incremented, it is necessary to check whether the word line or column select line address of the defect is already stored in the associated stack storage device. In this case, the counters are not activated since the defect is already repaired. This comparison must be made as early as in the first test pass because a pass is formed of a plurality of test patterns. This prevents a defect from being rectified by a plurality of redundant lines. The addresses of the lines having defect counters that have overflowed after the first test pass are stored in the word line stack storage device 41 or in the column select line stack storage device 42, respectively. In addition, the associated redundancy counters 32 are incremented. For this purpose, it is necessary to determine the domain of the line to be replaced, because there are usually a fixedly prescribed number of redundancy lines for each word line domain and for each column select line domain of a memory chip. The memory array 1 constitutes a memory region which in turn includes WL and CSL domains. The redundancy counters are advantageously constructed in such a way that an appropriate redundancy line is no longer present in the event of an overflow. The memory module is thus non-repairable and the test can be immediately ended in this case.

Detailed Description Text (10):
In this method too, a plurality of test passes are necessary for the selection of the lines to be repaired. This method differs from the first exemplary embodiment

in that in this concept the test sequence must be interrupted if a defect is identified. The defect address, that is to say the corresponding word line and column select line address, is then stored in the defect stack storage device. A comparator 22 subsequently checks to see whether or not the defect address is stored in one of several stack storage devices 41 . . . 43. Single-bit defects are stored in the storage device 43. If this is the case, then the test sequence is continued with another cell. Otherwise, an altered test sequence ensues. In this case, the number of all of the defects on the word line WL and on the column select line CSL of the original defect is determined separately. Before the defects are counted, it is necessary to check whether or not the additional defects have not already been rectified by the activation of a redundant line. The defect counters must be set to zero beforehand. Since, during the first comparison, it has been ascertained that both the address of the word line and the address of the column select line of the original defect have not yet been stored in a stack storage device, the following comparison operation can be simplified. In the event of a further defect on the word line of the original defect, only the stack storage device for the column select line addresses has to be examined. If an additional defect occurs on the column select line of the original defect, then only the stack storage device for the word line addresses has to be compared with the word line of the additional defect. If the number of defects exceeds a specific limit, then the. address of the line is stored in the corresponding stack storage device and the associated redundancy counter is incremented. The limit at which repair is intended to be effected is reduced in each following test pass.

Detailed Description Text (12):
The number of required test passes is also prescribed by the number of defect counters being used. If there are no further defects on the word line WL and the column select line CSL of the original defect, then what is involved is a single-bit defect, having an address which is stored in the stack storage device 43. The complete address, that is to say the word line and the column select line address, is stored in that storage device. This stack storage device is processed at the end of the built-in self-test. The defects stored therein can be replaced either by a redundant word line or by a redundant column select line. Since the redundant word lines are usually organized differently from the redundant column select lines, the test results differ depending on which redundancy lines have been used to rectify the single-bit defects. The complete test sequence is ended if there are no more required redundancy lines present or all of the defects have been rectified. If one of the redundancy counters overflows, then the memory chip is non-repairable and the test can be immediately terminated. The complete repair of the chip is identified by the fact that the counters always remain at zero throughout a test run. As soon as a defect counter is incremented, then the chip still has at least one defect and the test sequence cannot be ended in this case.

Detailed Description Text (13):
FIG. 3 illustrates a block diagram for explaining a third exemplary embodiment of the invention, which differs from the block diagram in FIG. 2 essentially by virtue of an additional buffer storage device 6. The major advantage of this concept is that only a single test pass is required for determining the word lines and column select lines to be replaced. In addition, the test sequence need not be altered, which would entail certain disadvantages. The defect addresses of the respective word line are stored in a buffer storage device. If a specific number of defects on this word line is exceeded, then the word line address is stored in the stack storage device 41 and the content of the buffer storage device is cleared. In addition, a corresponding redundancy counter 32 must be incremented. If the word line has fewer defects than the defined number of defects, then the complete content of the buffer storage device, that is to say all of the stored word line and column select line addresses, is written to the defect stack storage device 5 and the buffer store is subsequently cleared. The size of the defect stack storage device 5 influences the test results. While the next word line is being tested, that is to say the defect addresses are being determined and stored in the buffer